Claims

What is claimed:

1. An error detector comprising an input port adapted to receive encoded data and an error checking unit adapted to identify an error detection bit within the encoded data and to determining whether the error detection bit is valid.

2. The error detector according to claim 1, further comprising a data rate determination unit adapted to determine the data rate of the encoded data.

3. The error detector according to claim 2, wherein said error checking unit is adapted to use an output of said data rate determination unit in identifying the error detection bit.

4. There error detector according to claim 3, wherein said error detector is adapted to identify an error detection codeword within the encoded data.

5. The error detector according to claim 1, further comprising an error correction unit, said error correction unit adapted to modify the received data in accordance with a codeword within the encoded data.

6. A method comprising examining for an error detection bit a data block which is error correction coded.

7. The method according to claim 6, further comprising determining the validity of the error detection bit.

8. The method according to claim 7, further comprising determining the encoded block's data rate prior to examining the block for the error correction bit.

9. The method according to claim 8, wherein the block's data rate is factored into its examination.

10. The method according to claim 10, wherein the data block is mapped according to its data rate.

11. The method according to claim 6, wherein the data block is examined for an error detection codework.

12. A receiver comprising an error detection unit adapted to examine an error correction encoded data block for an error detection code bit, and a demapper operatively connected to said error detector for receiving the output of the detector.

13. The receiver according to claim 12, wherein the error detection unit is adapted to attempt to validate an identified error detection code bit.

14. The receiver according to claim 13, further comprising an error correction unit for altering the encoded data block in accordance with the error detection code bit.

15. The receiver according to claim 14, further comprising a decoder adapted to decode the encoded data block.

16. The receiver according to claim 15, wherein the decoder has error correction capabilities.

17. The receiver according to claim 12, further comprising a rate determination unit adapted to determine the encoded data blocks data rate.

18. The receiver according to claim 17, wherein the error detection unit receives data rate information from said data rate determination unit and examines the encoded data block in accordance with the data rate information.

19. The receiver according to claim 18, wherein the encoded data block is passed to said demapper when no errors are detected, to said error correction unit when errors are detected and the data block's data rate is greater than one half, and to said decoder when errors are detected and the data block's data rate is below one half.